AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-59. (Canceled)

60. (Currently Amended) A computer system for performing a fast Fourier transform on N ordered inputs in n stages comprising:

one or more vector processors configured as a non-final stage calculating means for repetitively performing in-place butterfly calculations for n-1 stages;

the one or more vector processors further configured as a final stage calculating means for performing a final stage of butterfly calculations including:

a first loop means for performing a portion of the final stage butterfly calculations, the first loop means performing a set of butterfly calculations, and storing butterfly calculation outputs in shuffled order in place of the selected inputs to result in a correct ordering of transform outputs; and

a second loop means for performing a remaining portion of the final stage butterfly calculations, the second loop means performing two sets of butterfly calculations, and storing butterfly calculation outputs from a first one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for a second one of the two sets of butterfly calculations and storing butterfly calculation outputs from the second one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for the first one of the two sets of butterfly calculations to result in a correct ordering of transform outputs,

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wherein the final stage calculating means performs all butterfly calculations as radix-4 butterflies having four inputs and four outputs

wherein N is a power of two, and

wherein the non-final stage calculating means performs a first stage of radix-8 butterfly calculations followed by n-2 stages of radix-4 butterfly calculations

wherein the computer system produces the correct ordering of transform outputs with no need to perform an additional bit-reversal ordering pass.

61. (Previously Presented) The computer system of claim 60, wherein the non-final and final stage calculating means include a four-fold single instruction multiple data (SIMD) processor for performing four radix-4 butterfly calculations at a time.

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